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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, May 2013
(2008 Scheme)
08.402 DIGITAL ELECTRONICS AND LOGIC DESIGN (E)

Time: 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. What are error correction codes ? Give example.
2. Convert $(ABC)_{16}$ to decimal.
3. Design and implement a half subtracter using NAND gates.
4. What are multiplexers ? Give example.
5. Differentiate between an edge triggered and a master slave flip flop.
6. What is a T flipflop ?
7. Draw the logic diagram of a mod 4 ripple down counter.
8. Explain fan out and power dissipation of TTL Logic family.
9. What is a PAL ?
10. Give any two applications of counters.

PART – B

Answer **any one** question from **each** Module. **Each** question carries **20** marks.

Module – I

11. a) Using K map reduce the expression, $f = \pi M (2, 8, 9, 10, 11, 12, 14)$ and implement the minimal expression in universal logic. **10**

    b) Explain the 2's complement method of arithmetic taking into account the various possibilities. Also give example for each condition. **10**

12. a) Convert the following :
    i) $(1101 . 11)_2$ to decimal
    ii) $(1762 . 46)_8$ to hexadecimal
    iii) $(76)_{10}$ to octal
    iv) $(E79A . 6A4)_{16}$ to binary. 10

    b) Prove the expression $(A + C)(\overline{A} + B) = AB + \overline{A}C$. 5

    c) State and explain De Morgan's theorems. 5

Module – II

13. a) Design and set up a 4 bit binary to gray code converter using gates. 10

    b) Design and set up a 4 bit BCD adder circuit using parallel binary adders. 10

14. a) Explain the internal circuit of a TTL NAND gate. 10

    b) Show an arrangement to obtain a 16 input multiplexer from two 8 input multiplexers. 10

Module – III

15. a) Explain a clocked SR flip flop with truth table. Also explain how it can be converted to a D flipflop. 12

    b) Explain a Universal Shift Register. 8

16. a) Write short notes on PLA and FPGA. 12

    b) Draw and explain the working of a Johnson's counter. 8